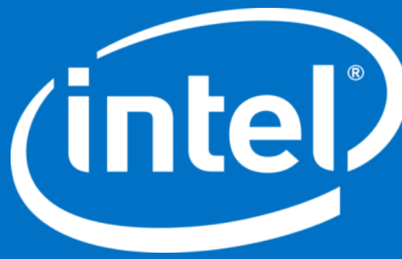


INVESTOR MEETING 2013

November 21, Santa Clara, CA

Advancing Moore's Law: Benefits Across the Portfolio

William Holt

Executive Vice President
General Manager, Technology and Manufacturing Group

INVESTOR MEETING 2013

November 21, Santa Clara, CA

Agenda

Fundamentals of Moore's Law
Cost, Capability, Performance/Watt

Reducing Cost in a Capital Intensive Environment

Applying the Benefits Across the Product Portfolio

Brief Update on14nm Status

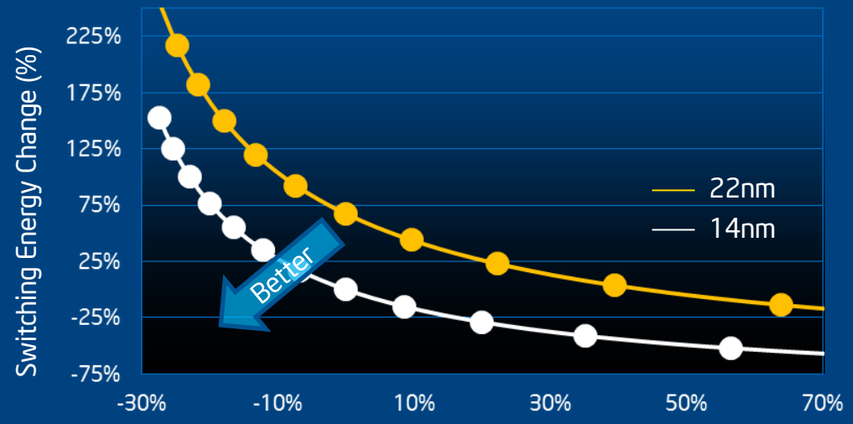
Yield

at the same point in development

Yield rapidly increasing, on track for matched yield in Q1 '14 *

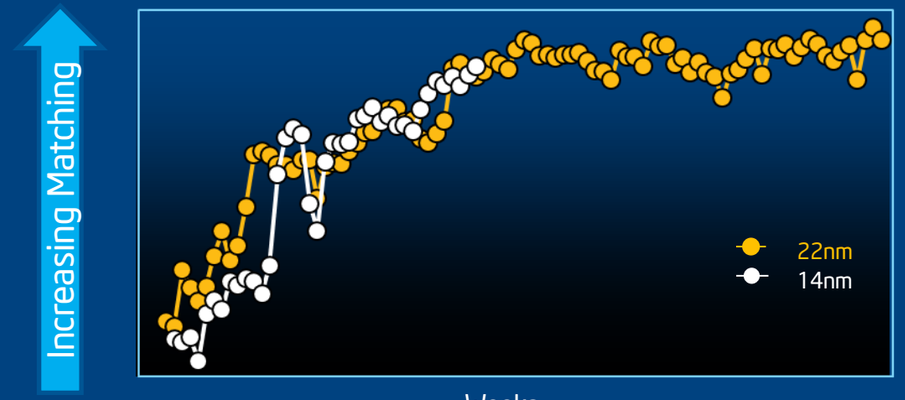
Performance Improvement

Switching Energy vs. Gate Delay



Key Parameter Matching

% of key process parameters meeting 3-sigma targets
at the same point in development



14 nm key process parameter matching on track with 22 nm trend

Reliability Scorecard

at the same point in development

Module	22nm (2 year offset)	14nm
Transistor		
Interconnect		
Thermo-Mechanical/Moisture		
Test Vehicle Yield		
ESD/LU		
Alpha Particle/Soft Error		

- Low risk: Meeting all cert goals
- Medium risk: Close to meeting goals
- High risk: Not yet meeting all goals, needs additional work

Generally healthy reliability at this stage, on track for Q1 '14 certification *

Source: Intel. * Forecast

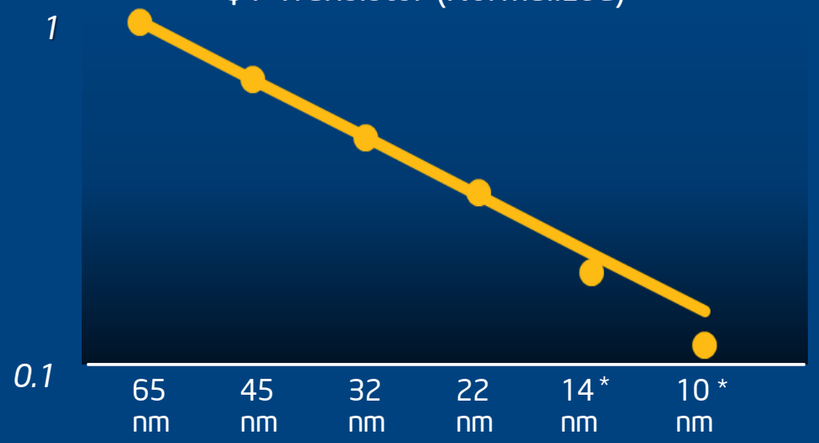
Fundamentals of Moore's Law

Reducing Cost in a Capital Intensive Environment

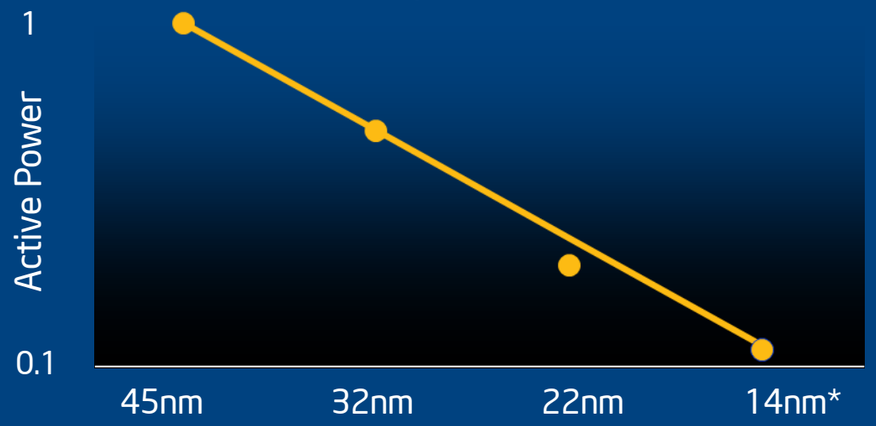
Applying the Benefits Across the Product Portfolio

Getting Benefits of Moore's Law Across all Value Vectors

Lower Cost

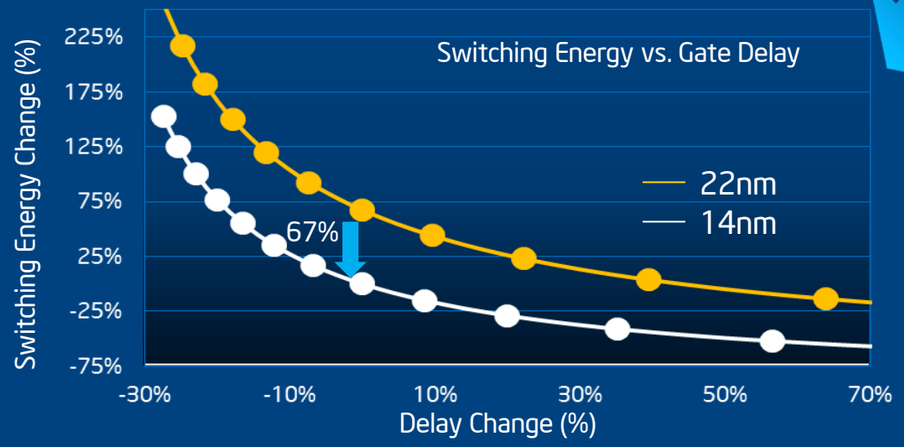


Active Power per Function

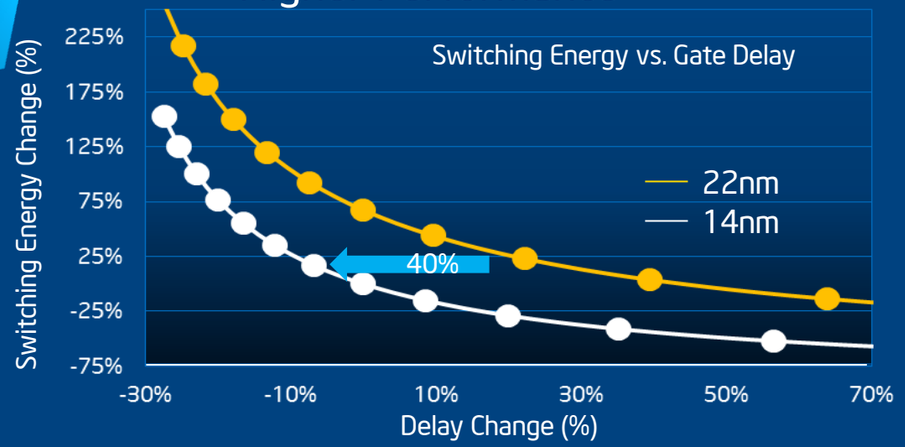


MOORE'S LAW

Lower Power



Higher Performance

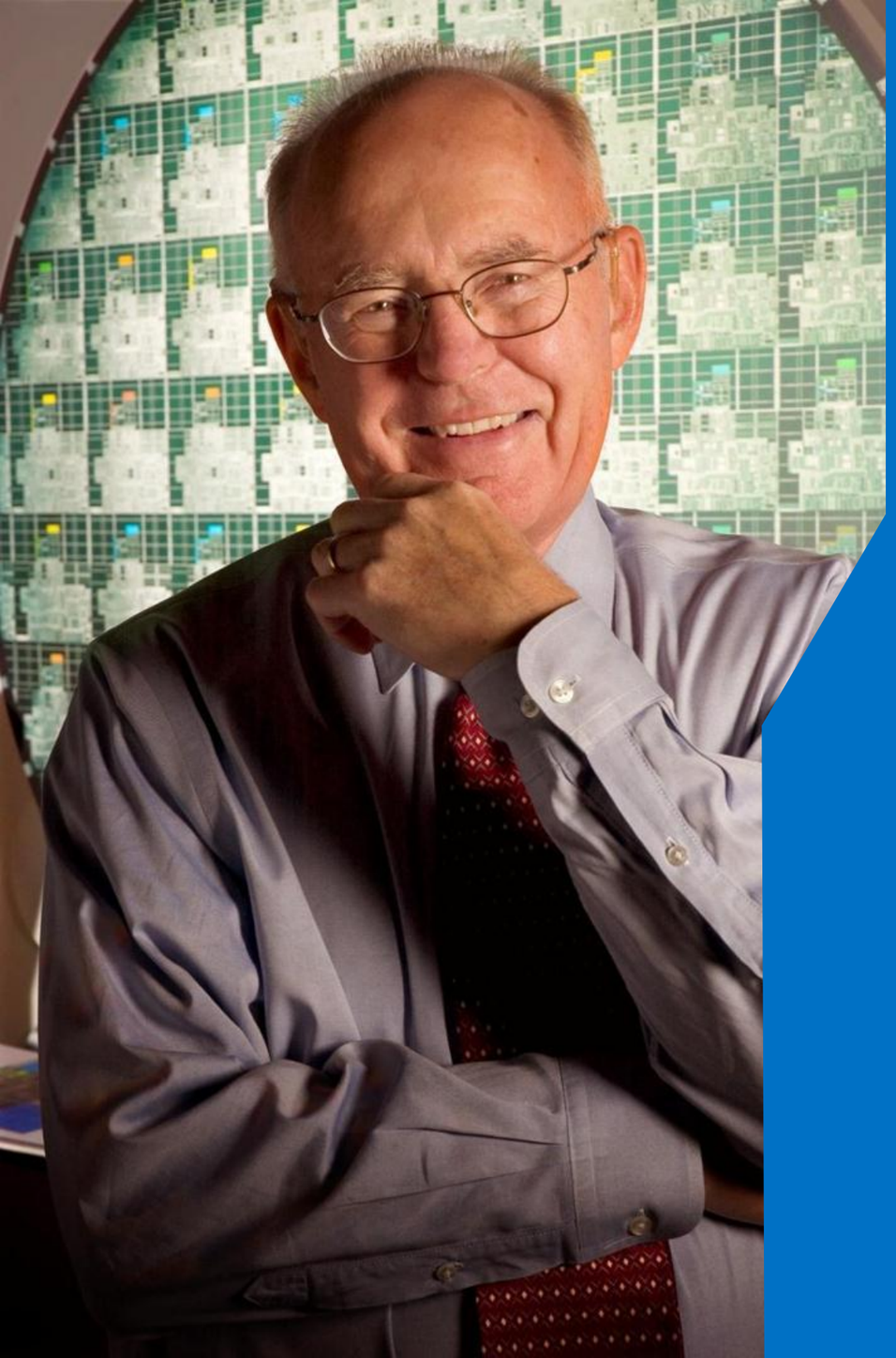


Source: Intel
* Forecast

Fundamentals of Moore's Law

Reducing Cost in a Capital Intensive Environment

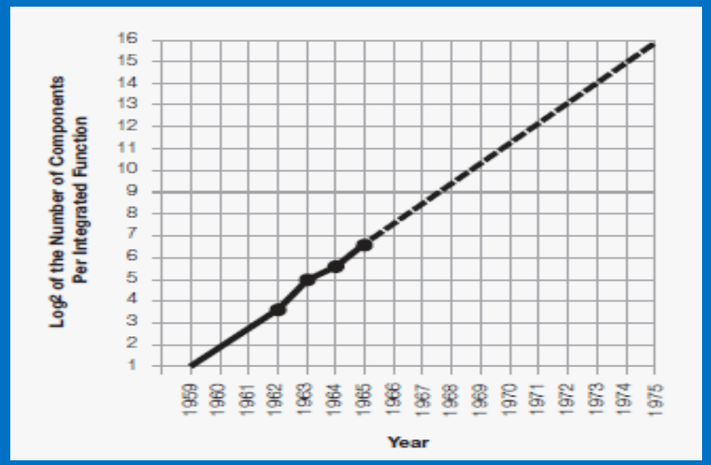
Applying the Benefits Across the Product Portfolio



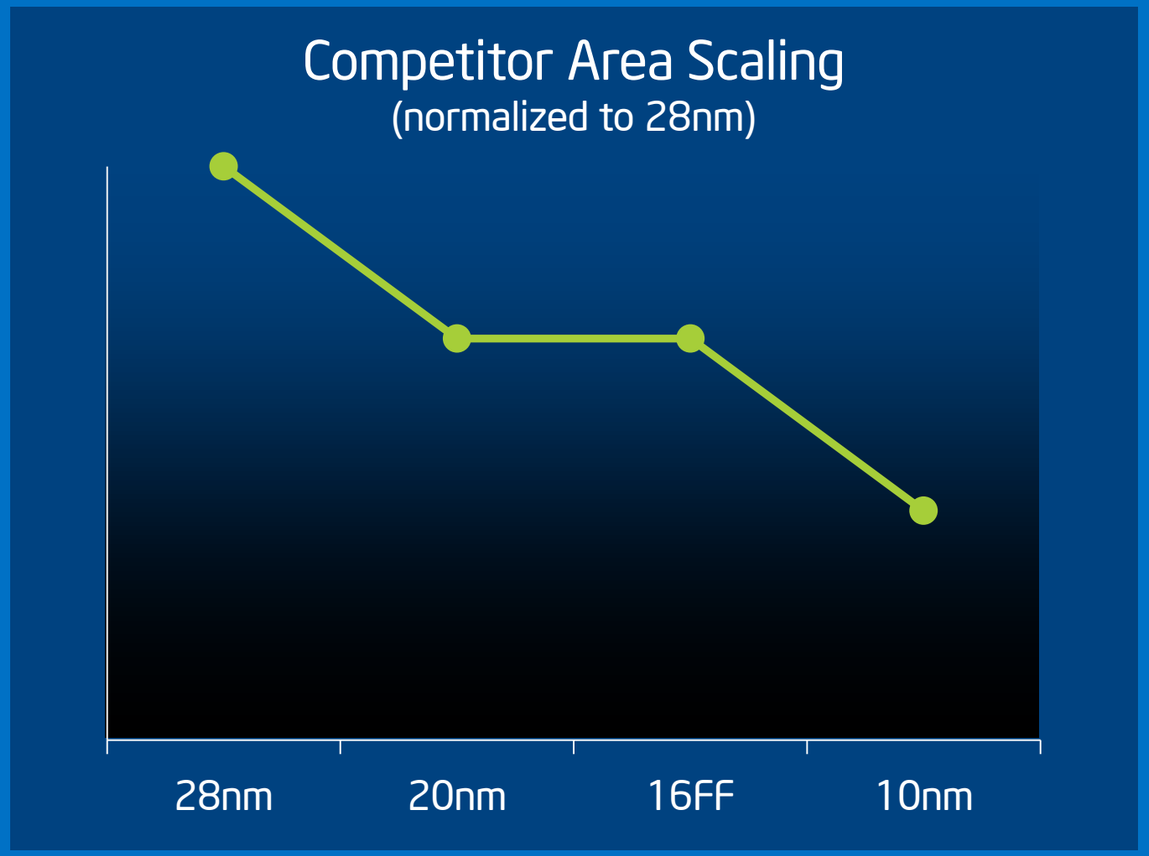
Moore's Law – It's All About Economics

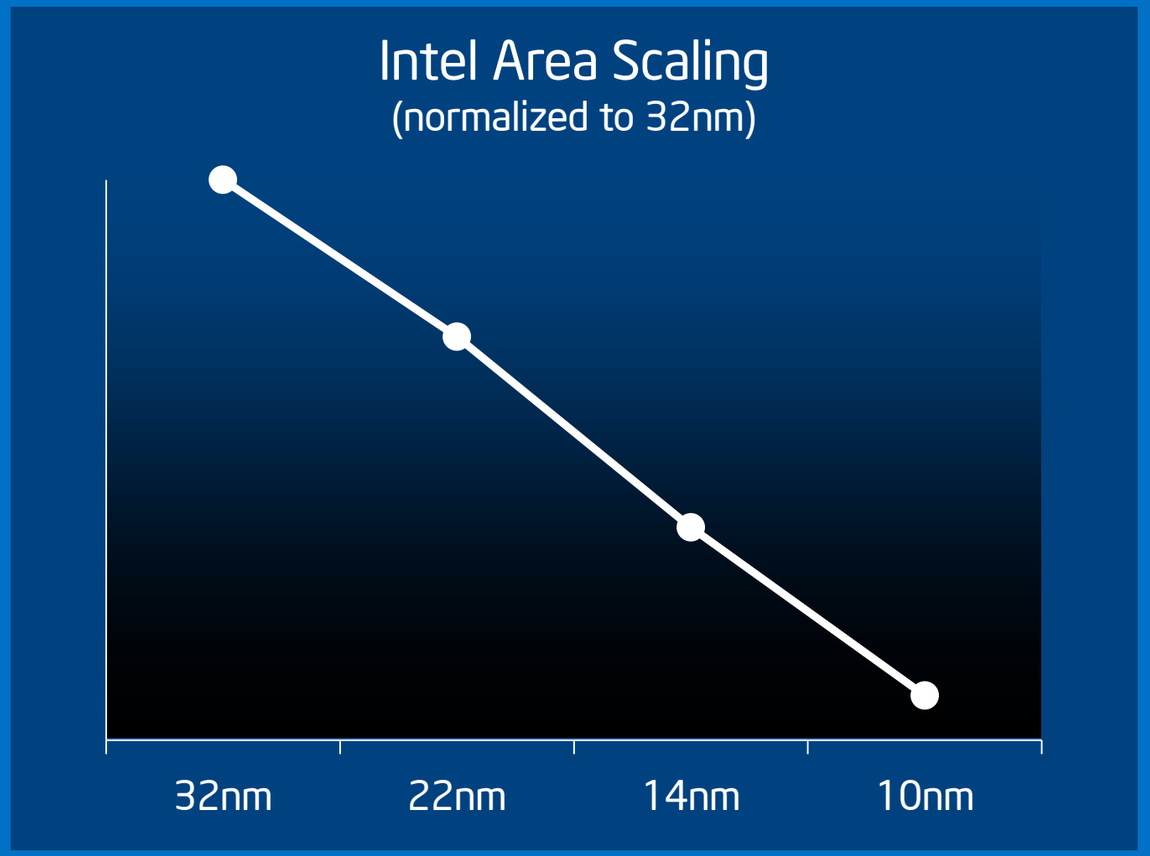
"**Reduced cost** is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."

Electronics, Volume 38, Number 8, April 19, 1965



Competitors Projecting No Chip Area Scaling





Competitor area scaling source: ARM Tech Con 2012, TSMC Keynote. Oct. 30, 2012 * Forecast

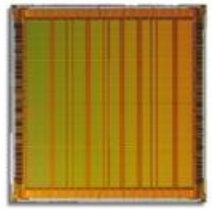
Intel is Continuing to Scale While Others are Pausing to do FinFETs

Our Customers See the Same Indicators

Altera vs. Xilinx Roadmap Comparison

Altera

TSMC "20 SoC"
20nm Planar



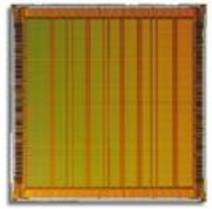
Significant shrink
& performance gain

Intel "14nm TriGate"
14nm FinFET

- *Higher Performance*
- *Lower Power*
- *Lower Cost*

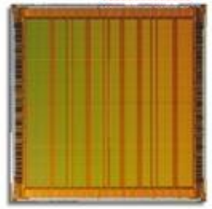
Xilinx

"20 SoC"
20nm Planar



Higher cost

"16FF"
20nm FinFET



Altera to capture high end FPGA market

Note: Altera relative die size estimates for equivalent capacity devices

ALTERA. MEASURABLE ADVANTAGE™

Stratix 10 Delivering the Unimaginable

Highest Performance FPGAs and SoCs

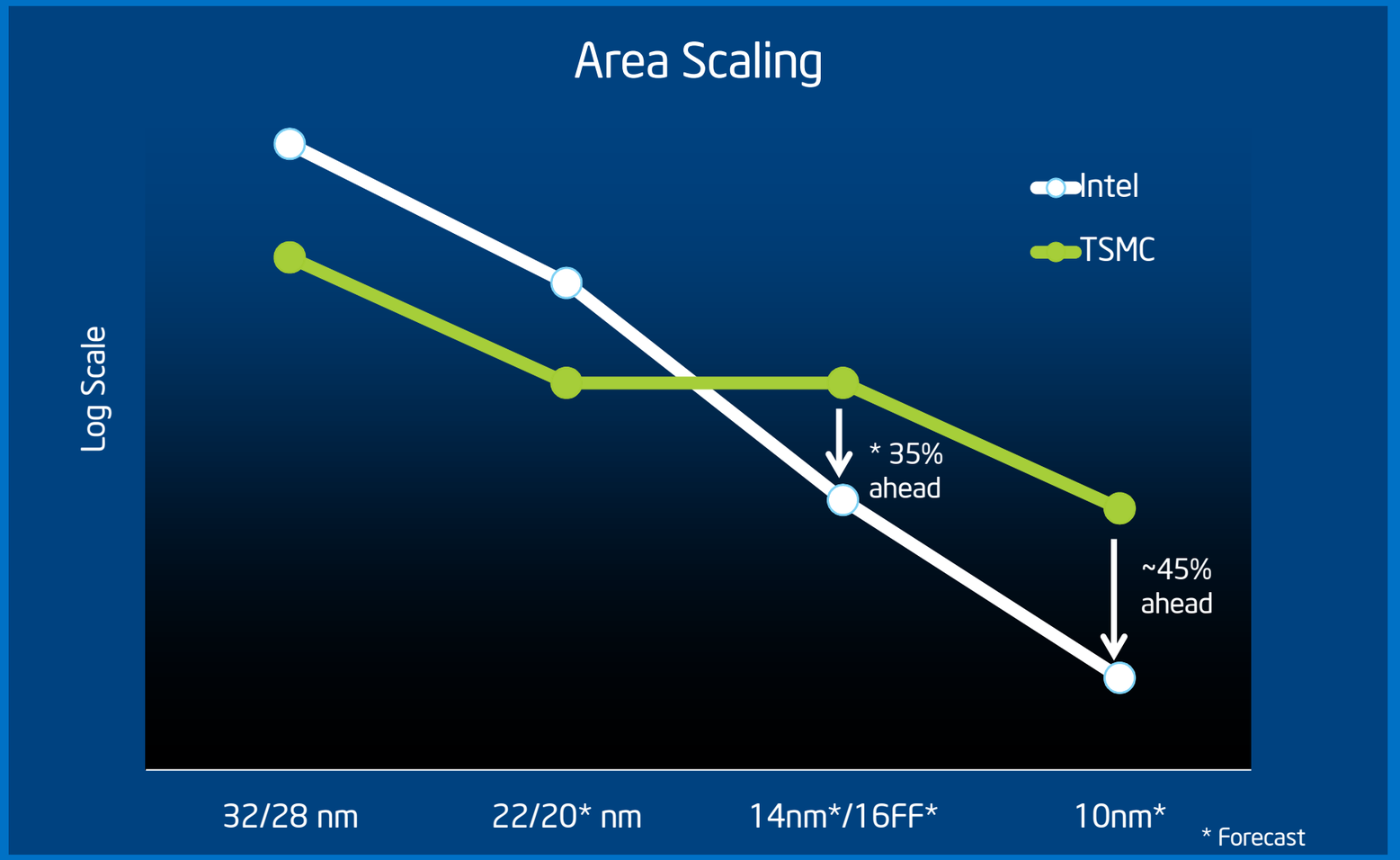
- **Intel 14 nm Tri-Gate process**

- **Enhanced high-performance architecture**

ALTERA. MEASURABLE ADVANTAGE™

Source: John Daane, CEO Altera @ CITI Global Technology Conference, Sep 4 2013

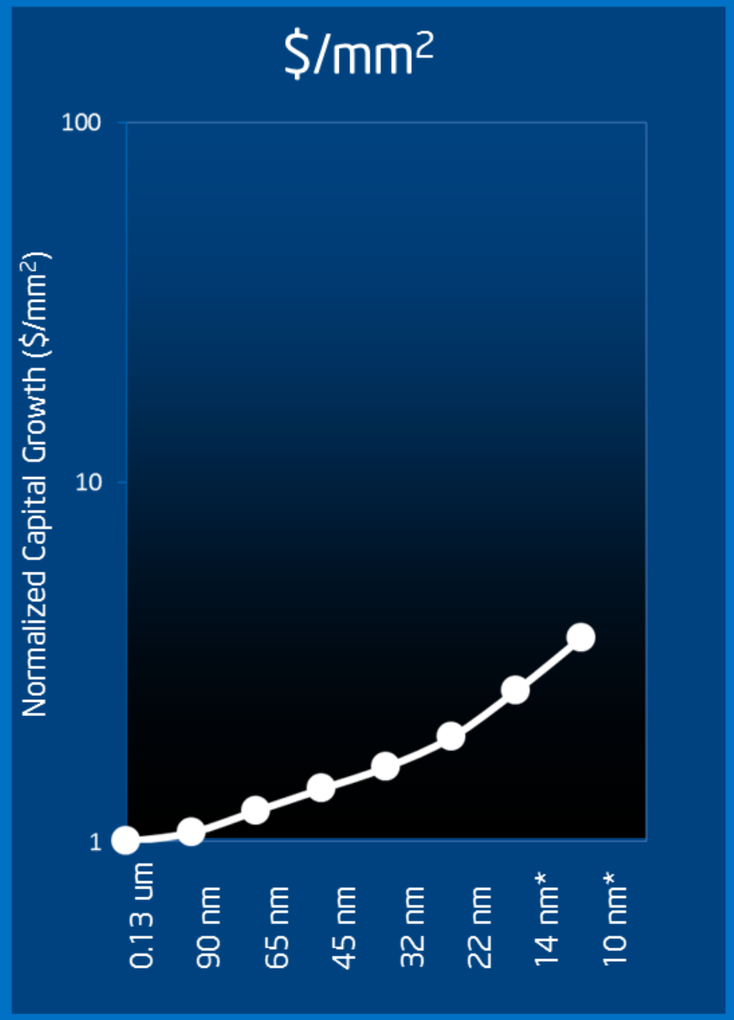
Intel Is Committed to Press Ahead on Density



Sources: TSMC keynote, ARM Tech Con 2012, Oct. 30, 2012. Intel data
Alignment based on internal assessment

Enables a "Transistor Like" Lead in Density

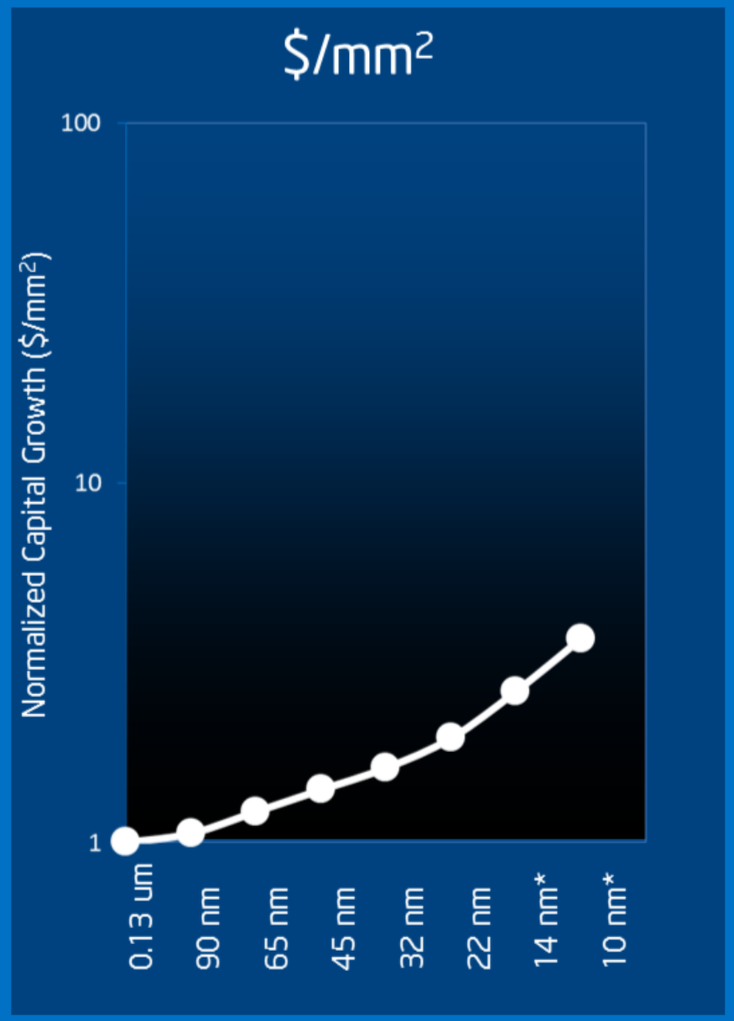
Density Improvements Offset Wafer Cost Trends



Source: Intel

* Forecast

Density Improvements Offset Wafer Cost Trends



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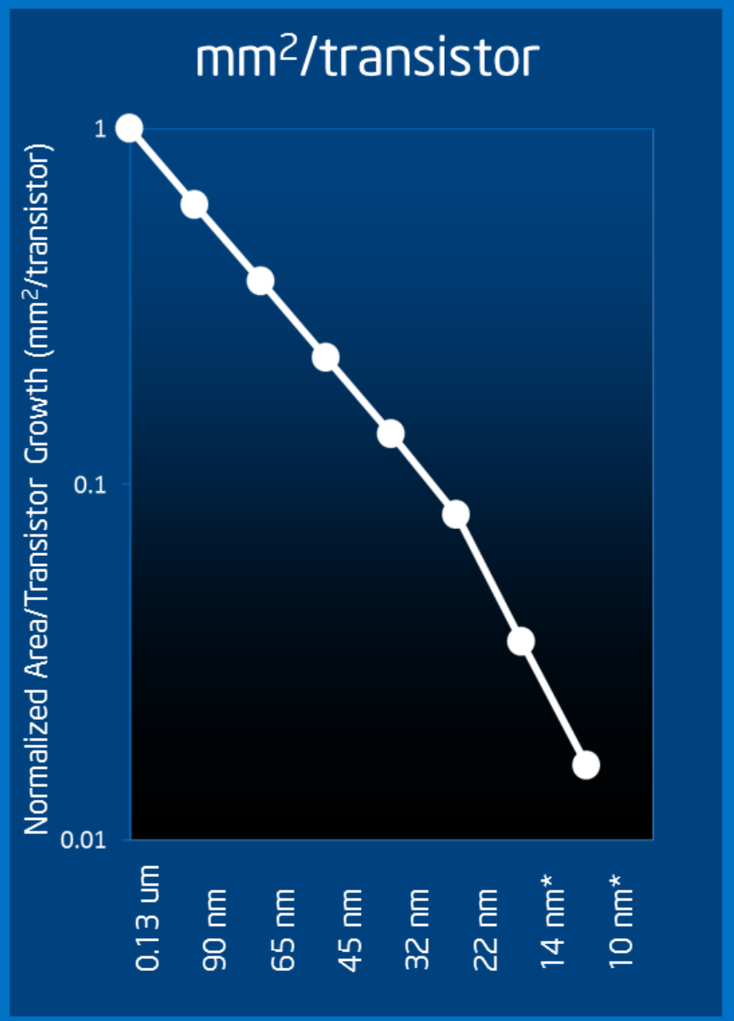
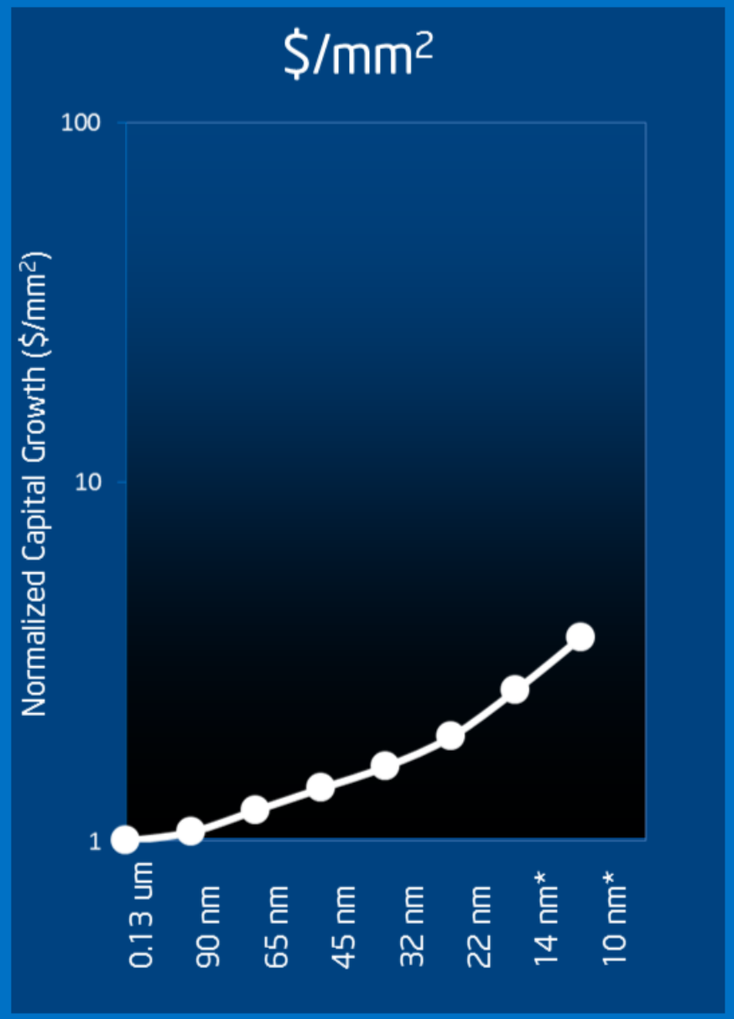


Source: Intel

* Forecast

Density Improvements Offset Wafer Cost Trends



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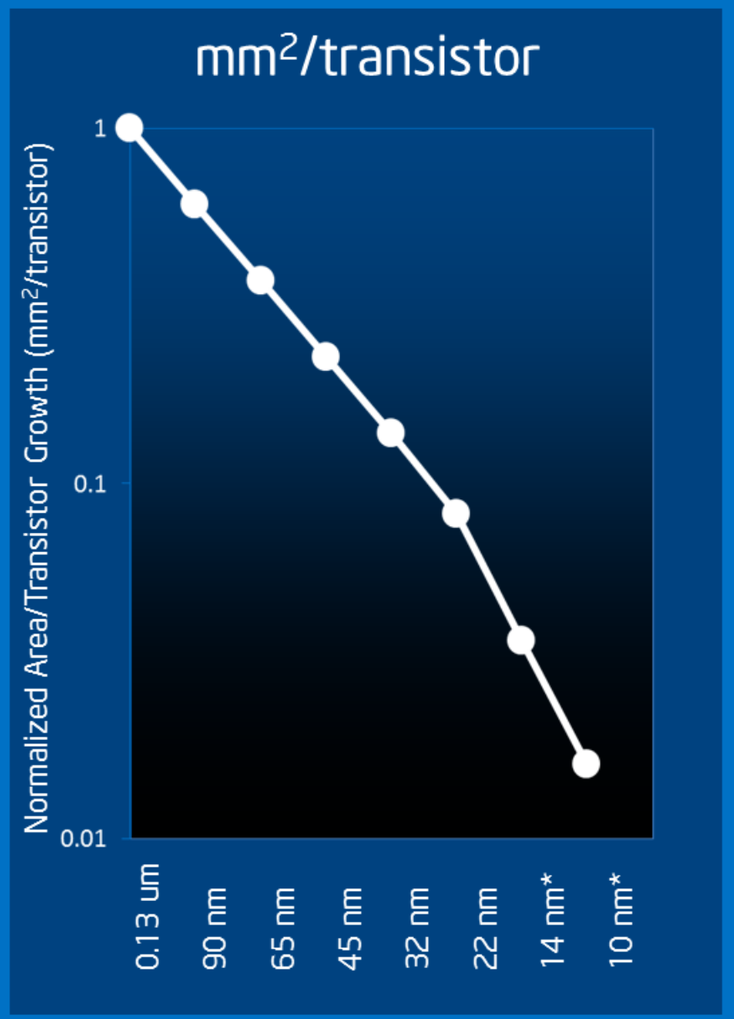

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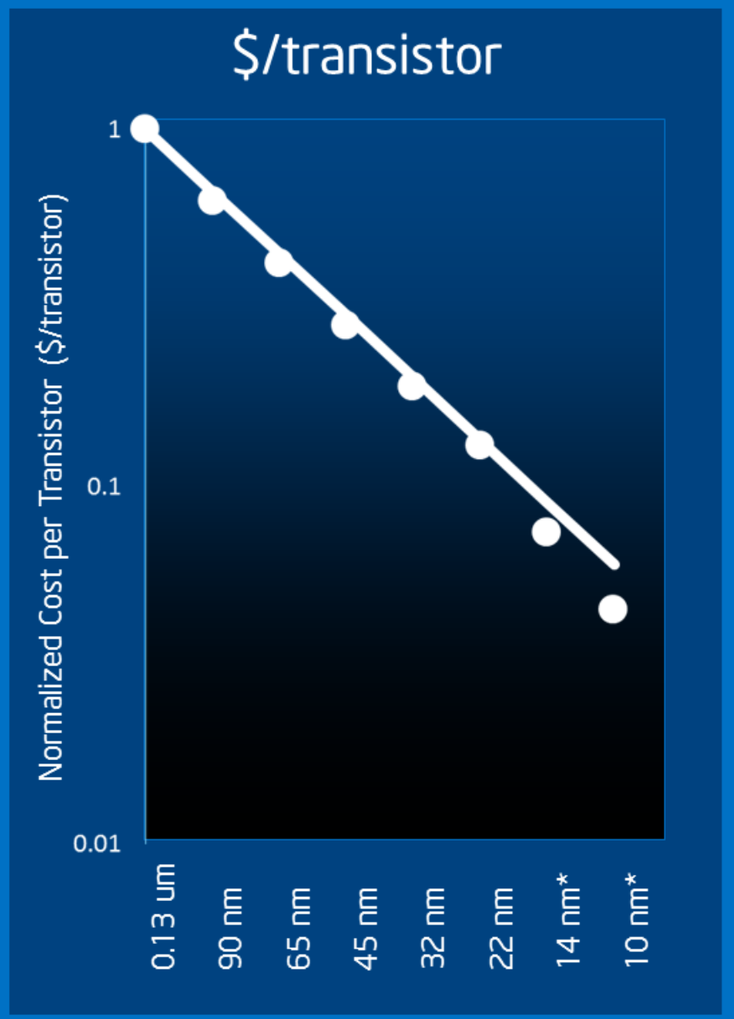
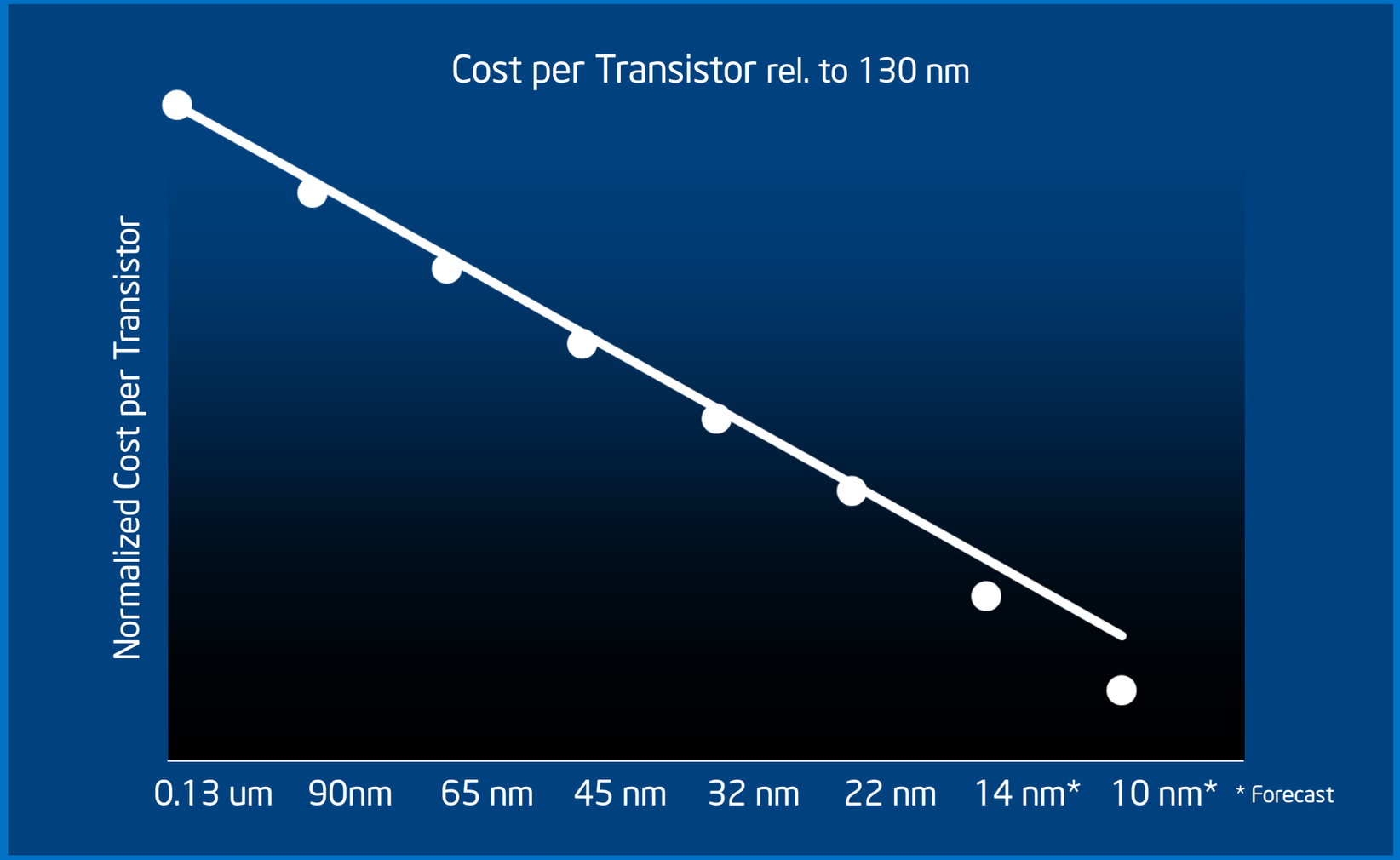


Source: Intel

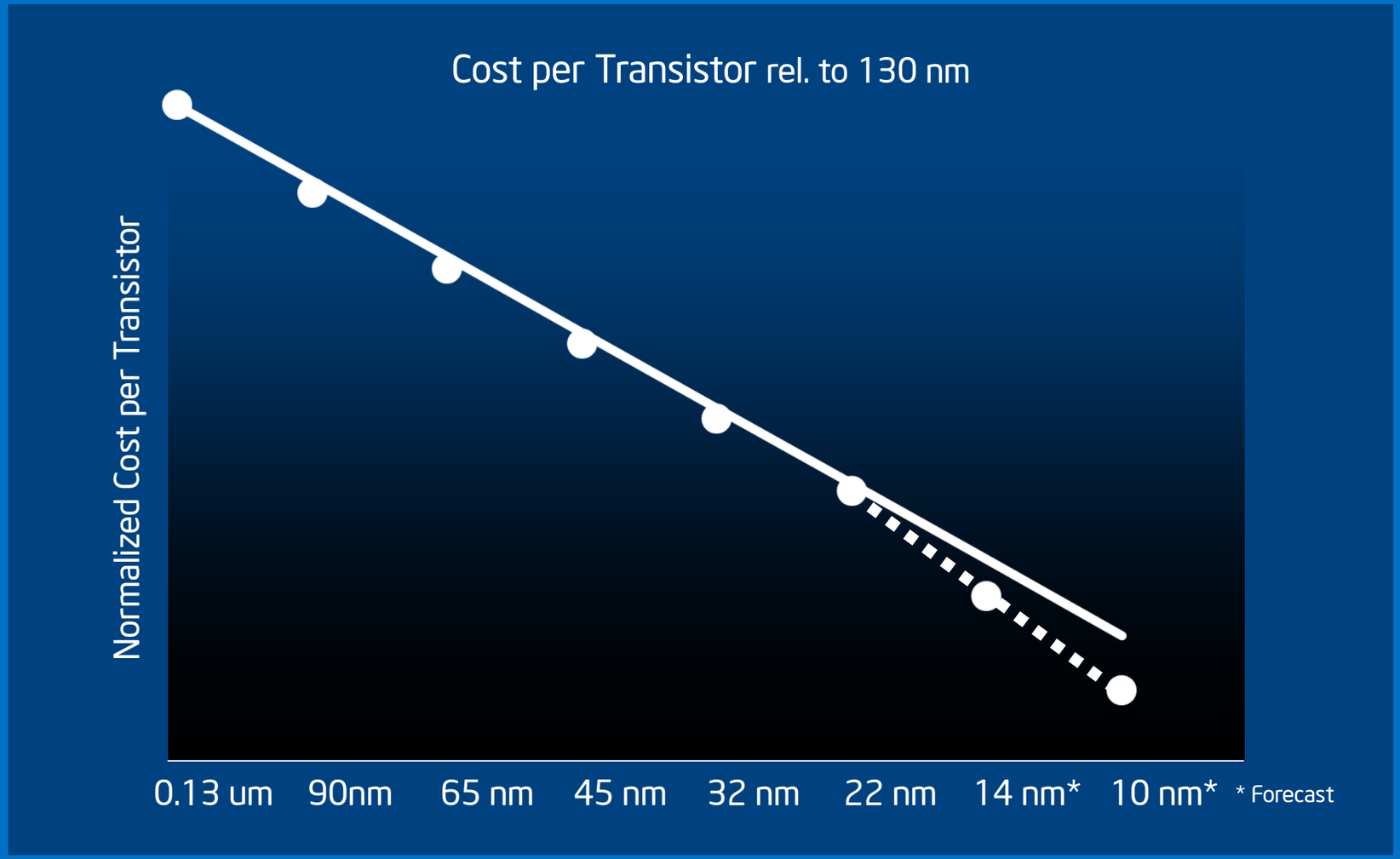
* Forecast

Density Scaling Continues Cost Improvement



Source: Intel

Density Scaling ~~Continues~~ Cost Improvement Accelerates



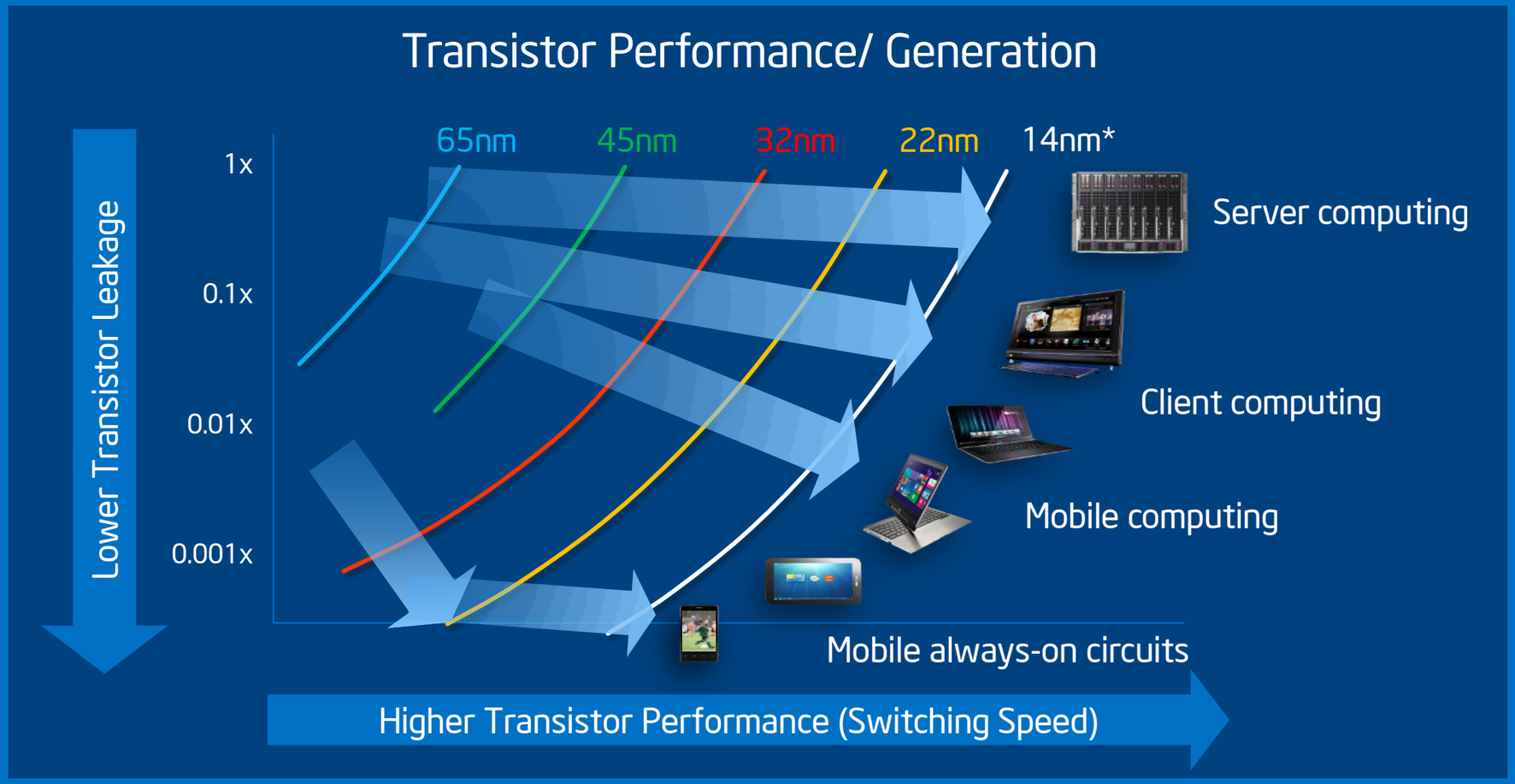
Source: Intel

Fundamentals of Moore's Law

Reducing Cost in a Capital Intensive Environment

Applying the Benefits Across the Product Portfolio

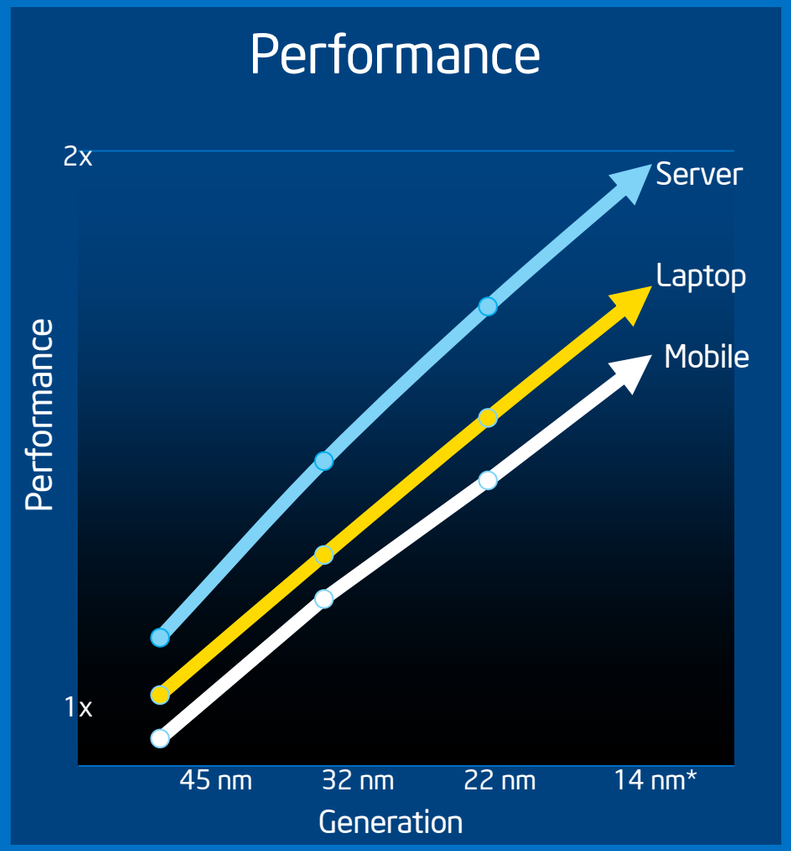
The Value of Better Transistors



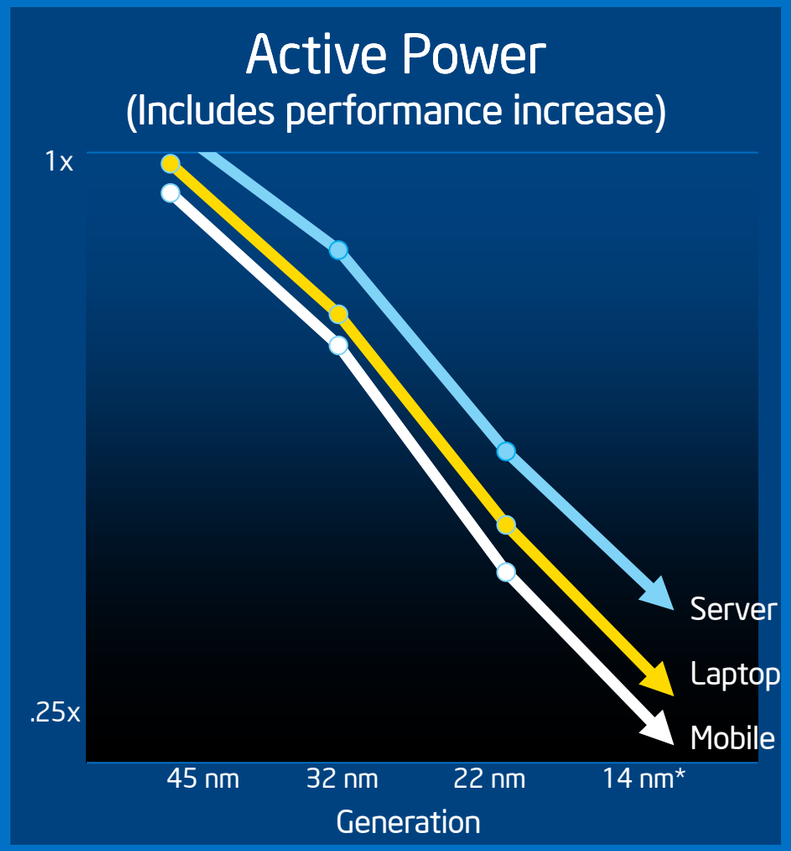
14nm: Continuing the Historical Gains

* Forecast
Source: Intel

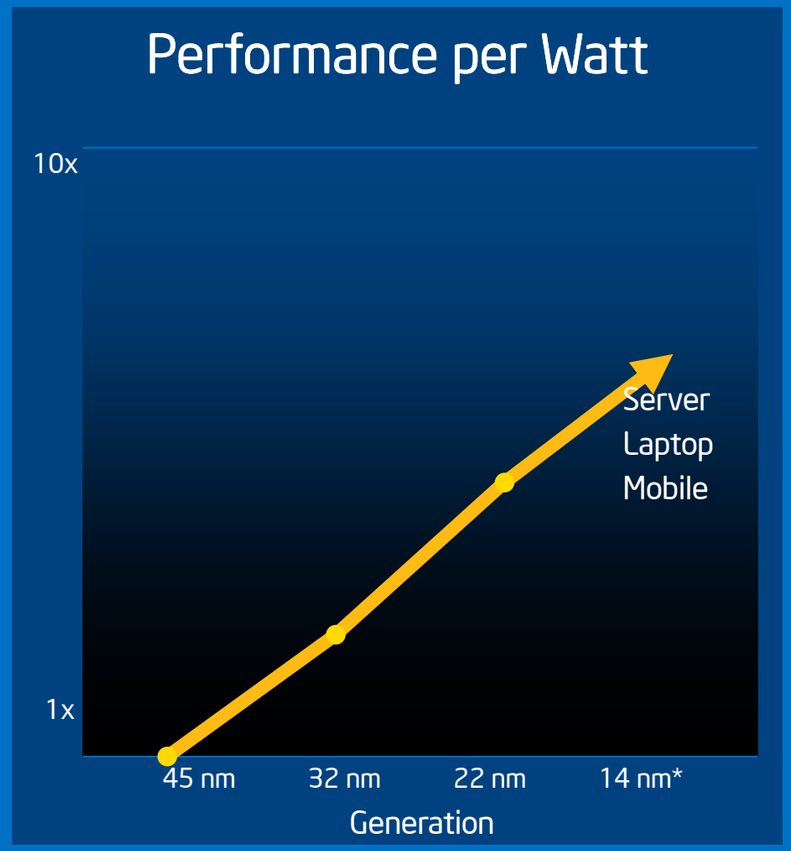
Different Improvement Focus for Different Segments



Performance Improved for All Product Families



Active Power Reduced for All Product Families

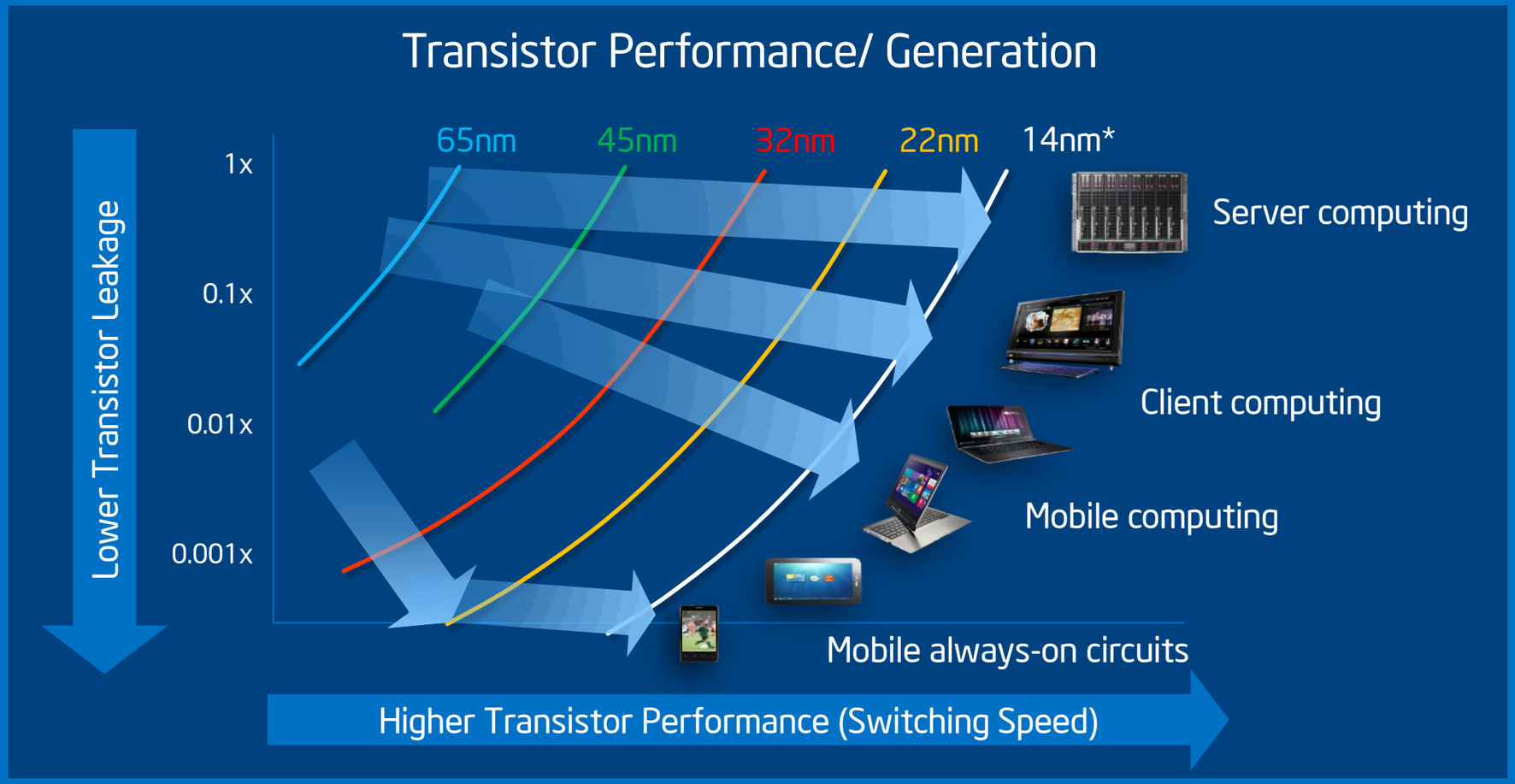


Performance per Watt Improves >1.6x per Generation

* Forecast
Source: Intel

Performance per Watt is the Critical enabler for all

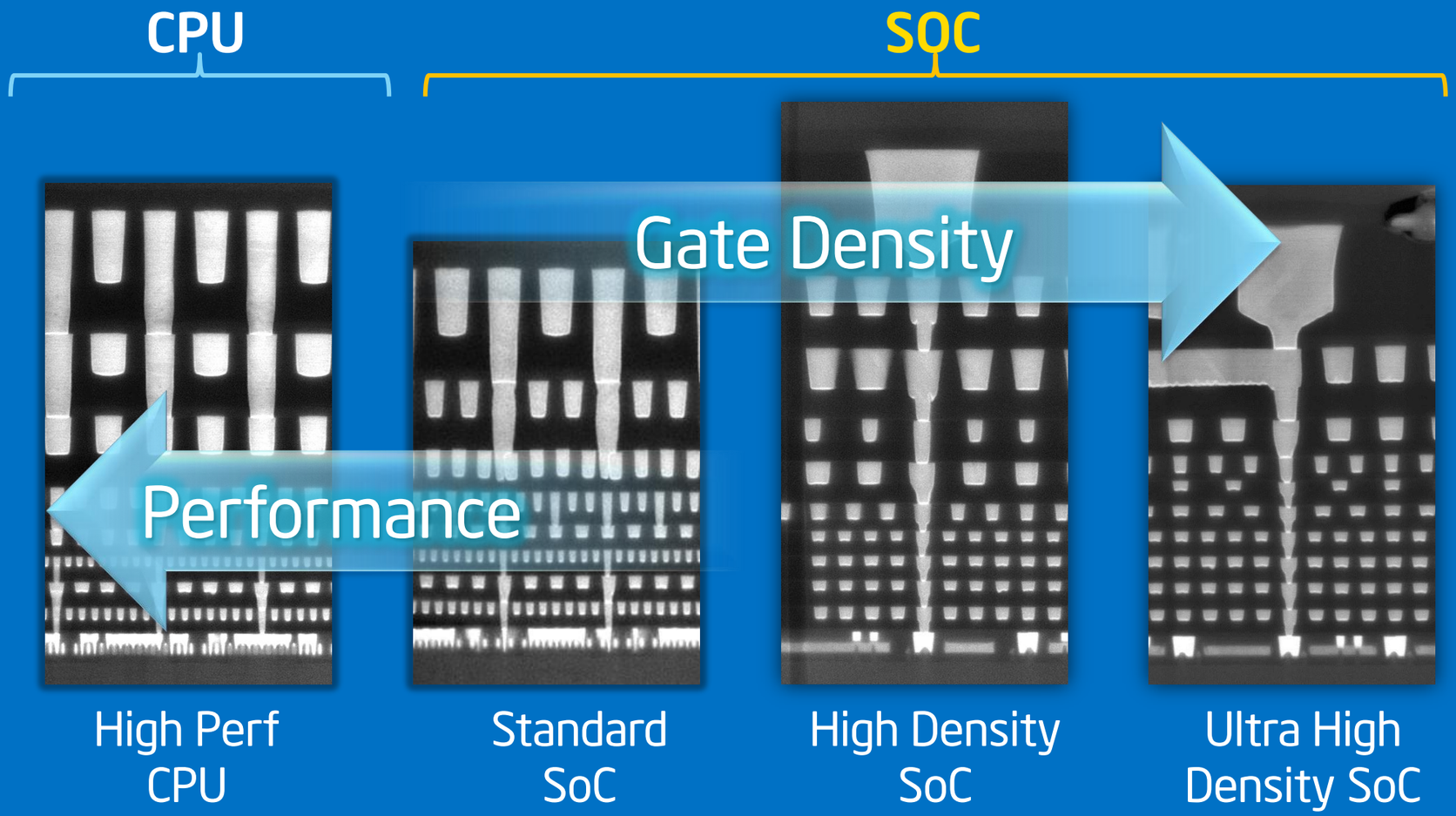
The Value of Better Transistors



The Same Fundamental Improvement Benefits a Wide Range of Products

* Forecast
Source: Intel

Interconnects Options Enable Product Optimization

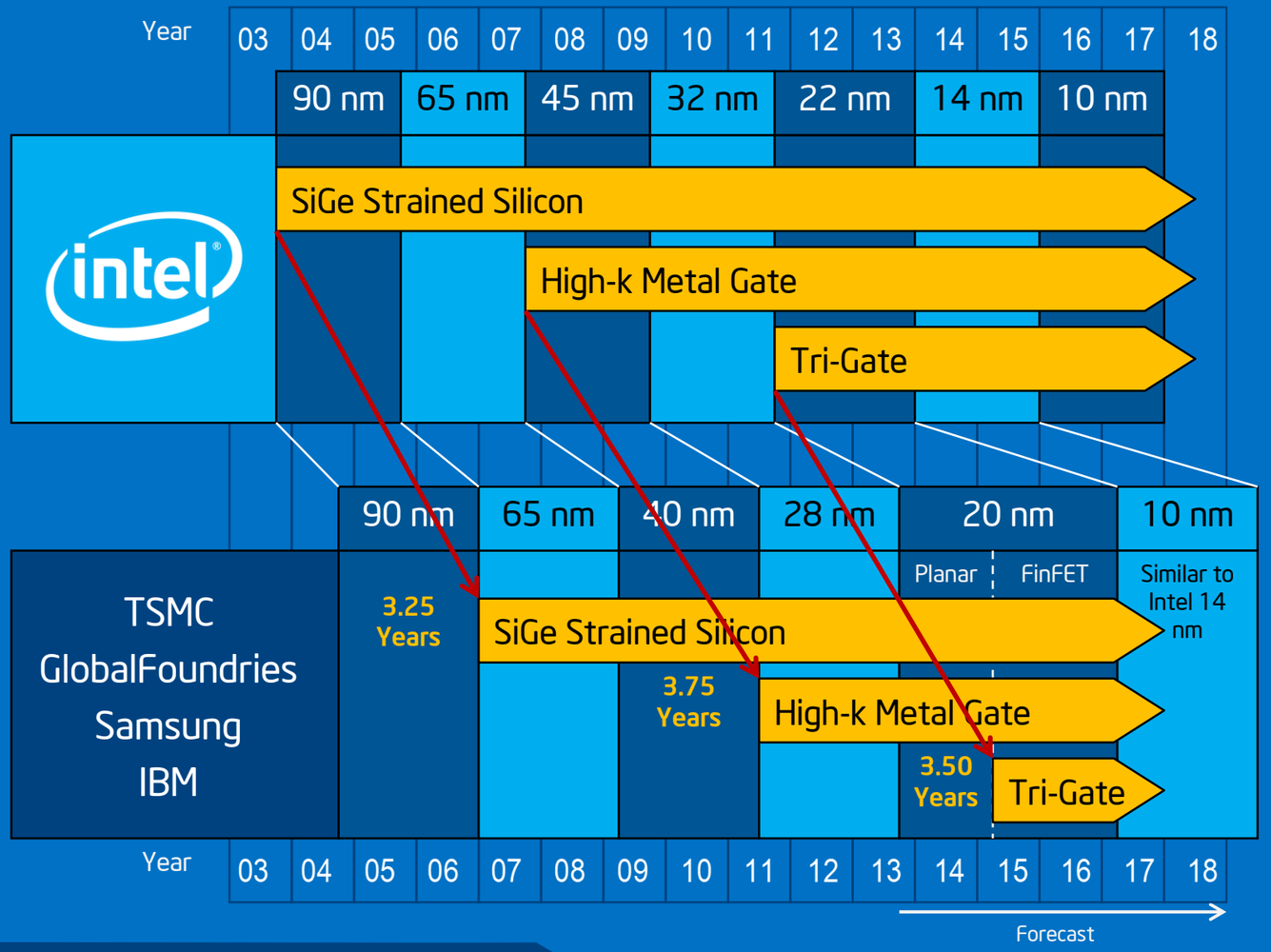


CPU Interconnects Focused on Performance
SoC Interconnects Focused on Density

Expanding the Breadth of Technology Options

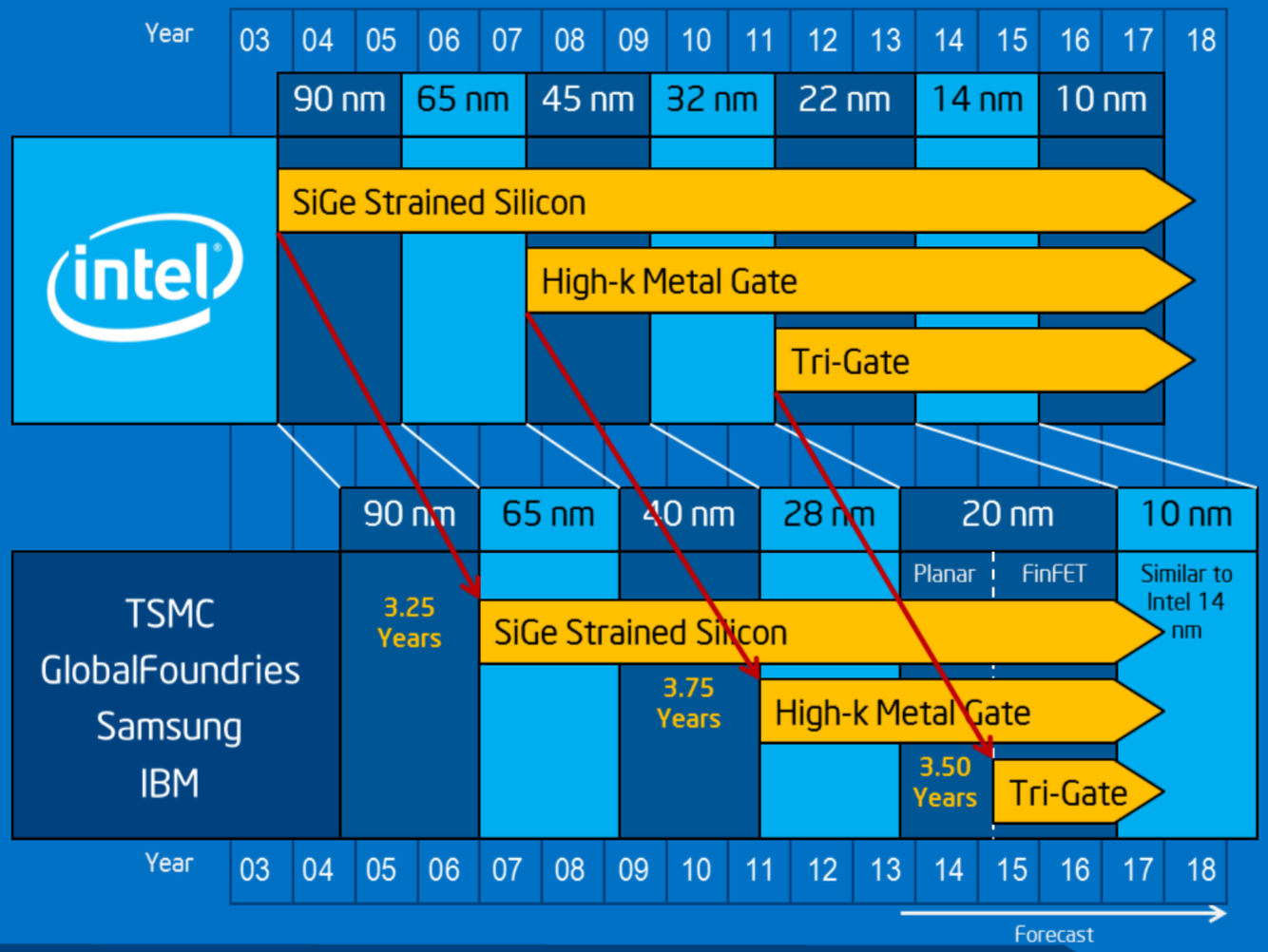
		Intel					Intel Custom Foundry		
Features	**Options**	Client/ Server	Chipsets	Tablets	Embedded DRAM	Wireless Products	Smart Phones	Entry Mobile	FPGA/ ASIC
Logic Transistor	HP - High Perf.	●							●
	SP – Std. Perf/Pwr		●	●	●	●	●	●	●
	LP - Low Power		●			●	●	●	
I/O Transistor	1.2V	●				●	●		●
	1.8V			●	●	●	●	●	●
	3.3V		●						
Interconnect	RC Performance	●							
	High Density		●	●			●		●
	Low Cost					●		●	
	COB				●				
Embedded Memory	e-SRAM – High Performance	●							●
	e-SRAM – Low Voltage	●	●	●				●	
	e-SRAM – Low Power		●			●	●		
	e-SRAM – Dual Port								●
	e-PROM/OTP	●	●	●	●	●	●	●	●
	e-DRAM				●				
Basic Analog/ Passives	Resistor - Linear	●	●	●	●	●	●	●	●
	Capacitor – MOS, MFC	●	●	●	●	●	●	●	●
	Capacitor - MIMCAP	●		●			●		●
	Inductor - Standard	●		●		●		●	●
Library	High Performance	●							●
	General Purpose	●	●	●	●		●	●	●
	High Density		●	●		●	●	●	●
Adv. Mixed Signals/ RF	**Transistor – PA**					●			
	Resistor - Precision		●	●		●	●	●	●
	Capacitor - Linear					●			
	Inductor – High Q					●			
	Deep Nwell/Triple Well					●			
	High Res Substrate					●			

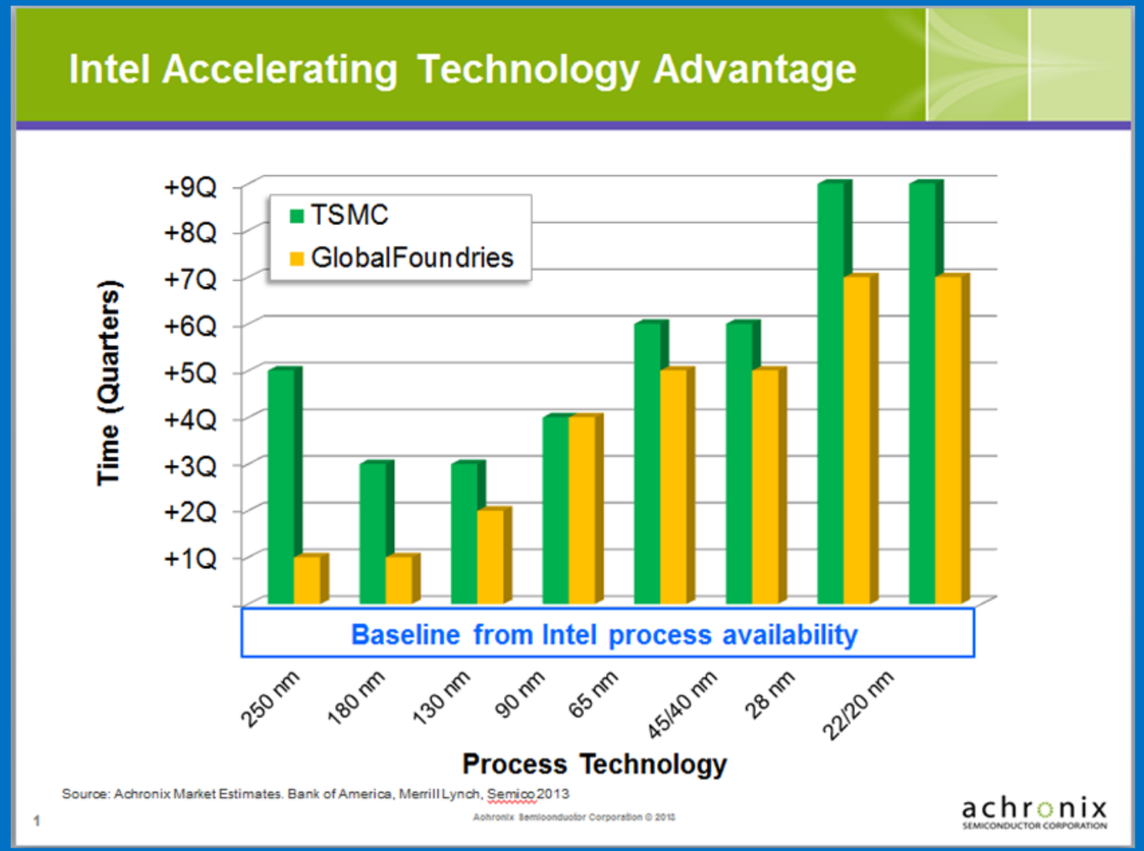
Intel Technology Leadership



Intel Has ~3.5 Year Lead In Introducing Revolutionary Transistor Technologies

Intel Technology Leadership





Source: Achronix, *Leading the Industry ,Achronix Now Shipping Intel 22nm FPGAs,* November 7th, 2013

Intel Has ~3.5 Year Lead In Introducing Revolutionary Transistor Technologies

Summary

Intel Continues to Deliver the Benefits of Moore's Law

True Cost Reduction Remains Possible in a Capital Intensive Environment

The Benefits of Technology Apply Across the Product Portfolio

Risk Factors

The above statements and any others in this document that refer to plans and expectations for the fourth quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel’s actual results, and variances from Intel’s current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company’s expectations. Demand could be different from Intel’s expectations due to factors including changes in business and economic conditions; customer acceptance of Intel’s and competitors’ products; supply constraints and other disruptions affecting customers; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel’s results, including revenue, gross margin, expenses and interest and other, would likely be adversely affected in the event of widespread financial and business disruption on account of a default by the U.S. on U.S. government obligations and/or a prolonged failure to maintain significant U.S. government operations. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel’s products; actions taken by Intel’s competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel’s response to such actions; and Intel’s ability to respond quickly to technological developments and to incorporate new features into its products. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; segment product mix; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. The tax rate expectation is based on current tax law and current expected income. The tax rate may be affected by the jurisdictions in which profits are determined to be earned and taxed; changes in the estimates of credits, benefits and deductions; the resolution of issues arising from tax audits with various tax authorities, including payment of interest and penalties; and the ability to realize deferred tax assets. Gains or losses from equity securities and interest and other could vary from expectations depending on gains or losses on the sale, exchange, change in the fair value or impairments of debt and equity investments; interest rates; cash balances; and changes in fair value of derivative instruments. Intel’s results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. 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